

REMARKS

Status of the Claims

Claims 22-43 are pending, with Claims 22, 38, and 39 being independent. Claims 22, 24, 27, 38, and 39 have been amended and Claims 41-43 have been added. Support for the amendments can be found throughout the application and support for the new claims can be found, for example, at page 8, lines 10-17. No new matter has been added.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the foregoing amendments and following remarks.

Form PTO-892

Applicant respectfully requests correction of the Form PTO-892 attached to the Office Action mailed on September 9, 2004, which incorrectly lists U.S. Patent No. 5,922,673 to Gluckman et al., instead of U.S. Patent No. 5,292,673 to Shinriki et al.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 22-40 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,091,763 (“Sanchez”) and further in view of U.S. Patent No. 5,880,508 (“Wu”) and U.S. Patent No. 5,322,809 (“Moslehi”). Applicant respectfully disagrees with the rejection; therefore, this rejection is traversed.

Sanchez is cited as allegedly disclosing an interfacial layer on a silicon semiconductor substrate; a gate electrode of an electrically conductive material; a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; source and drain regions that are adjacent the gate electrode; a pair of spacers formed adjacent to the gate electrode; and a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions. However, as explained below, Sanchez discloses conductive spacers formed over a gate oxide layer adjacent to the edges of the inner gate member and that a thin oxide spacer between the inner gate member and the conductive spacers may additionally be provided.

Wu is cited as disclosing a high dielectric constant layer, that comprises a material of Ta₂O₅, wherein the interfacial layer comprises silicon nitride or silicon oxynitride and a barrier layer between the gate electrode and the high dielectric constant layer. The Office Action alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wu with Sanchez, because the high dielectric constant layer provides for a gate insulator layer that reduces hot carrier effect and the barrier layer helps to provide better adhesion between the high dielectric constant layer and the gate.

Moslehi is cited as disclosing a planar interlayer insulator and silicide on the source and drain regions. The Office Action further alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moslehi with Sanchez, because the silicide on the source and drain provides for a lower resistivity for better

electrical conduction for metal contact and the planar insulator keeps topography level so preceding layers can be uniform.

Sanchez discloses a high speed submicron transistor which exhibits a high immunity to hot electron degradation and is viable for VLSI manufacturing. (Abstract). Sanchez discloses polysilicon or TiN conductive spacers formed over a gate oxide layer adjacent to the edges of the inner gate member, which together with the inner gate member form the gate for the transistor. (Column 4, Lines 2-7). Sanchez further discloses that a thin oxide spacer between the inner gate member and the conductive spacers may additionally be provided. (Column 5, Lines 62-68).

Wu discloses a transistor formed on a semi-conductor substrate, where the transistor includes a gate dielectric layer formed on the semi-conductor substrate. (Abstract).

Moslehi discloses a self-aligned silicide process that enables different silicide thicknesses for polysilicon gates and source/drain junction regions. (Abstract).

In contrast, Claim 22 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5 , $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1,

and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; (f) a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and (g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

Claim 38 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon nitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5 , $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; (f) a

pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and (g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

Claim 39 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon oxynitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5 , $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_{s-s}-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; (f) a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and (g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or

in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143.

Applicant respectfully submits that Sanchez further in view of Wu and Moslehi does not teach or suggest all the claim limitations. In particular, Applicant respectfully submits that the combination of Sanchez, Wu, and Moslehi is not suggestive of the combination of features recited in claims 22, 38, and 39, each of which includes a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer and a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

As noted above, Sanchez discloses conductive spacers formed over a gate oxide layer adjacent to the edges of the inner gate member, which together with the inner gate member form the gate for the transistor, and that a thin oxide spacer between the inner gate member and the conductive spacers may additionally be provided. The Office Action asserts that the gate oxide layer of Sanchez is analogous to the presently claimed interfacial layer. (Page 2).

In contrast, as disclosed in the present application, first spacers are formed by depositing a phosphosilicate glass (PSG) film over the entire surface of the device and then anisotropic etching the glass. The spacers can also be made from oxides or nitrides. (Page 8, Lines 10-13). After formation of the first spacers, the exposed high dielectric constant

material is removed, with the remaining layer of high dielectric material serving as the gate oxide. (Page 8, Lines 10-16). Second spacers are then formed by the same procedure as for the first spacers. (Page 8, Lines 16-17). Thus, since the exposed high dielectric constant material was removed after formation of the first spacers, the second spacers are adjacent to the high dielectric constant layer. Further, the second spacers are formed on the interfacial layer, as recited in new claims 41-43.

Accordingly, the combination of Sanchez, Wu, and Moslehi discloses a thin oxide spacer between the inner gate member and *conductive spacer formed over the gate oxide layer*, rather than a first pair of *non-conductive spacers formed on the high dielectric constant layer* adjacent to the gate electrode and a second pair *non-conductive spacers that are adjacent to the high dielectric constant layer* and the first spacers. As the prior art references when combined do not teach or suggest all the claim limitations, a *prima facie* case of obviousness has not been established. Withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing amendments and remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

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